AMENDMENTS TO THE CLAIMS

1-11. (Canceled).

12. (Previously Presented) An input/output (I/O) device for use in a process control system for providing communications between a process controller and a field device, the process control system including a plurality of I/O devices in communication with the process controller using a bus, the I/O device comprising:

a first interface directly coupled to the bus for communicatively linking the I/O device with the process controller via the bus wherein the process controller produces a control message for receipt by the field device, the first interface adapted to receive the control message from the process controller for the field device via the bus, wherein the field device controls a physical process control parameter or measures a physical process control parameter;

a second interface for communicatively linking the I/O device with the field device apart from the bus; and

a device processor coupled with the first interface for controlling operation of the I/O device including performing fault detection for the I/O device;

wherein the device processor, upon detection of a potential device fault, severs the communication link provided by the first interface with the bus.

13. (Previously Presented) The I/O device of claim 12 wherein the bus includes a data line and the first interface communicatively links the I/O device with the data line of the bus, and wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the data line.

14. (Previously Presented) The I/O device of claim 13 wherein the I/O device further comprises a relay coupled between the device processor and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and the data

line of the bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state.

15. (Original) The I/O device of claim 13 wherein the data line of the bus is a data line capable of being affected by the I/O device.

16. (Previously Presented) The I/O device of claim 15 wherein the data line of the bus is at least one of a transmit data line and a clock data line.

17. (Previously Presented) The I/O device of claim 13 further comprising a driver device coupled between the device processor and the first interface, the driver device having a driver output coupled to the first interface and readable by the processor, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the data line, performs further fault detection on the I/O device by forcing states to the driver output, and determines a device fault responsive to readings from the driver output.

18. (Previously Presented) The I/O device of claim 12 wherein the bus includes a plurality of data lines, and the first interface communicatively links the I/O device to the plurality of data lines, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the plurality of data lines of the bus.

19. (Original) The I/O device of claim 12 wherein the fault detection is an initial fault detection, and further comprising a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed.

20. (Original) The I/O device of claim 19 wherein the later fault detection is performed in a similar manner to the initial fault detection.

21. (Previously Presented) The I/O device of claim 12 wherein the potential device fault includes the I/O device prohibiting other I/O devices utilizing the bus from

communicating over the bus, and the device processor severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

22. (Previously Presented) The I/O device of claim 21 wherein the bus includes at least one data line and the first interface communicatively links the I/O device with the at least one data line of the bus, and the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus includes the I/O device affecting the bus by the I/O device transmitting an undesired signal on the at least one data line of the bus, where the device processor severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

23. (Previously Presented) The I/O device of claim 12 wherein the device processor fault detection includes the device processor attempting to affect the bus using the first interface, wherein the device processor detects the potential device fault by an inability of the device processor to affect the bus.

24. (Original) The I/O device of claim 23 wherein the device processor attempting to affect the bus includes the device processor attempting to change the state of the bus.

25. (Original) The I/O device of claim 24 wherein the device processor attempting to change the state of the bus includes the device processor forcing a state on the bus.

26. (Original) The I/O device of claim 25 wherein the device processor forcing the state of the bus includes the device processor transmitting one of a digital high value and a digital low value on the bus.

27. (Original) The I/O device of claim 23 further comprising the device processor reading the bus after attempting to affect the bus, wherein the device processor determines the inability to affect the bus using the reading of the bus.

28. (Previously Presented) The I/O device of claim 12 further comprising the device processor performing further fault detection upon severing of the communication link, wherein when the device processor detects no device fault from the further fault detection, the device processor reestablishes the communication link with the bus.

29. (Original) The I/O device of claim 12 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising the I/O device being assigned to one of the synchronous time slots, where the device processor performs fault detection during the asynchronous time slot following the corresponding synchronous time slot.

30. (Original) The I/O device of claim 12 wherein the device processor performs the fault detection when the I/O device is not transmitting I/O device information on the bus.

31-36. (Canceled).

37-54. (Canceled).

55. (Canceled).

56. (Previously Presented) A method for severing communication between an input/output (I/O) device and a bus in a process control system, the process control system including a plurality of I/O devices communicatively linked with a process controller using the bus, the method comprising:

providing a first interface directly coupled to the bus for communicatively linking the I/O device with the process controller via the bus wherein the process controller produces a control message for receipt by a field device, the first interface adapted to receive the control message from the process controller for the field device via the bus or to provide one or more field device messages from the field device to the process controller, wherein the field device

controls a physical process control parameter or measures a physical process control parameter;

providing a second interface for communicatively linking the I/O device with the field device apart from the bus;

performing fault detection by a device processor of the I/O device; and

severing the communication link provided by the first interface when the device processor detects a potential device fault in the I/O device.

57. (Previously Presented) The method of claim 56 wherein the bus includes a data line, and:

providing the first interface includes providing the first interface for communicatively linking the I/O device with the data line; and

severing of the communication link includes severing the communication link provided by the first interface with the data line when the device processor detects a potential device fault in the I/O device.

58. (Previously Presented) The method of claim 57 further comprising:

providing a relay device between the device processor and the first interface, the relay communicatively linking the I/O device with the data line in a first state, and severing the communicative link between the I/O device and the data line of the bus in a second state;

wherein the severing of the communication link provided by the first interface includes actuating the relay to the second state by the device processor.

59. (Previously Presented) The method of claim 57 wherein severing of the communication link provided by the first interface with the data line includes severing the communication link provided by the first interface with a data line capable of being affected by the I/O device.

60. (Previously Presented) The method of claim 59 wherein severing of the communication link provided by the first interface with the data line includes severing the communication link provided by the first interface with at least one of a transmit data line and clock data line.

61. (Previously Presented) The method of claim 57 further comprising:

providing a driver device between the device processor and the first interface, the device driver having a driver output coupled to the first interface and the device processor; and

performing further fault detection on the I/O device by forcing states to the driver output and reading the state of the driver output by the device processor upon severing the communication link with the first interface;

wherein determining of the device fault includes determining of the device fault responsive to the reading of the state of the driver output.

62. (Previously Presented) The method of claim 56 wherein the bus includes a plurality of data lines, and further including;

providing the first interface includes providing the first interface communicatively linking the I/O device to the plurality of data lines,

wherein the severing of the communication link includes severing the communication link provided by the first interface to the plurality of data lines of the bus upon detection of a device fault.

63. (Previously Presented) The method of claim 56 wherein the fault detection is an initial fault detection, and further comprising:

performing a later fault detection by the I/O device after the communicative link from the I/O device and the bus is severed.

64. (Original) The method of claim 63 wherein the performing the later fault detection includes performing the later fault detection in a similar manner as the initial fault detection.

65. (Original) The method of claim 63 further comprising reestablishing the communication link with the bus by the device processor when the later fault detection detects no I/O device fault.

66. (Original) The method of claim 56 wherein the performing the fault detection includes attempting to affect the bus using the communicating link, wherein the potential device fault is detected by an inability to affect the bus.

67. (Original) The method of claim 66 wherein the attempting to affect the bus includes attempting to change the state of the bus.

68. (Original) The method of claim 67 wherein the attempting to change the state of the bus includes forcing a state on the bus.

69. (Original) The method of claim 68 wherein the forcing the state of the bus includes forcing the bus to one of a digital high value and a digital low value.

70. (Original) The method of claim 56 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising assigning the I/O device to one of the synchronous time slots, wherein the performing of the fault detection by the device processor includes performing the fault detection during the asynchronous time slot following the corresponding synchronous time slot which the I/O device is assigned.

71. (Original) The method of claim 56 wherein the performing of the fault detection by the device processor includes performing the fault detection when the I/O device is not transmitting I/O device information on the bus.

72-79. (Canceled).

80. (Previously Presented) An apparatus for use in a process control system, the process control system including a process controller adapted to produce a control message for receipt by a field device, the process controller in communication with a plurality of devices using a bus, the apparatus being an input/output (I/O) device and comprising:

a first interface directly coupled to the bus for communicatively linking the apparatus with the process controller via the bus, the first interface adapted to receive the control message from the process controller for a field device via the bus or to provide one or more field device messages from the field device to the process controller, the field device being coupled to the apparatus through a second interface apart from the bus, wherein the field device controls a physical process control parameter or measures a physical process control parameter; and

a processor coupled with the first interface for controlling operation of the apparatus including performing fault detection for the apparatus;

wherein the processor, upon detection of a potential apparatus fault, severs the communication link provided by the first interface with the bus.

81-86. (Canceled).

87. (Canceled)

88. (Previously Presented) The apparatus of claim 80 wherein the bus includes a data line and the first interface communicatively links the apparatus with the data line of the bus, and wherein the processor, upon detection of the potential apparatus fault, severs the communication link provided by the first interface with the data line.

89. (Previously Presented) The apparatus of claim 88 wherein the apparatus further comprises a relay coupled between the processor and the data line of the bus, the relay having a first state communicatively linking the apparatus with the data line, and a second state severing the communicative link between the apparatus and the data line of the bus, wherein the processor, upon detection of the potential apparatus fault, severs the communication link with the bus by actuating the relay to the second state.

90. (Previously Presented) The apparatus of claim 88 wherein the data line of the bus is a data line capable of being affected by the apparatus.

91. (Currently Amended) A process control system, comprising:

a bus;

a process controller communicatively coupled to the bus; and

a plurality of I/O devices coupled to the bus for providing communications between the process controller and a plurality of field devices, wherein each I/O device includes a first interface directly coupled to the bus for communicatively linking the I/O device to the bus, the first interface adapted to receive ~~the~~ a control message from the process controller for a field device of the plurality of field devices via the bus or to provide one or more field device messages from the field device to the process controller, wherein the field device controls a physical process control parameter or measures a physical process control parameter; and

a device processor coupled with the first interface for controlling operation of the I/O device including performing fault detection for the I/O device, and, upon detection of a potential I/O device fault, severing the communication link provided by the first interface with the bus.

92. (Previously Presented) The system of claim 91 wherein each I/O device of the plurality of I/O devices further comprises a second interface for coupling the I/O device to the plurality of field devices.

93. (Previously Presented) The system of claim 92 wherein the at least one of the plurality of field devices is a sensor or a valve.

94. (Previously Presented) The system of claim 91 wherein the bus includes a data line and the first interface of each I/O device communicatively links the I/O device with the data line of the bus, and wherein the device processor of each I/O device, upon detection of the potential device fault, severs the communication link provided by the first interface of the I/O device with the data line.

95. (Previously Presented) The system of claim 94 wherein each I/O device further comprises a relay coupled between the device processor of each I/O device and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and

the data line of the bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state.

96. (Previously Presented) The system of claim 94 wherein the data line of the bus is a data line capable of being affected by each of the plurality of I/O devices.

97. (Previously Presented) The system of claim 96 wherein the data line of the bus is at least one of a transmit data line for transmitting field device information from each of the plurality of I/O devices to the controller, and a clock data line.

98. (Previously Presented) The system of claim 94 wherein each of the plurality of I/O devices further comprises a driver device coupled between the device processor and the first interface, the driver device having a driver output coupled to the first interface and readable by the processor, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the first interface with the data line, performs further fault detection on the I/O device by forcing states to the driver output, and determines a device fault responsive to readings from the driver output.

99. (Previously Presented) The system of claim 91 wherein the bus includes a plurality of data lines, and the first interface of each of the plurality of I/O devices communicatively links the I/O device to the plurality of data lines, wherein the device processor of the I/O device, upon detection of the potential device fault, severs the communication link provided by the first interface with the plurality of data lines of the bus.

100. (Previously Presented) The system of claim 91 wherein the fault detection is an initial fault detection, and further comprises a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed.

101. (Previously Presented) The system of claim 100 wherein the later fault detection is performed in a similar manner to the initial fault detection.

102. (Previously Presented) The system of claim 91 wherein the potential device fault includes one of the plurality of I/O devices prohibiting another of the plurality of I/O devices utilizing the bus from communicating over the bus, and the device processor of the one of the I/O devices severing the communication link with the bus allows the other I/O devices to communicate over the bus.

103. (Previously Presented) The system of claim 91 wherein the fault detection of the device processor includes the device processor attempting to affect the bus using the first interface, wherein the device processor detects the potential device fault by an inability of the device processor to affect the bus.

104. (Previously Presented) The system of claim 103 wherein the device processor attempting to affect the bus includes the device processor attempting to change the state of the bus.

105. (Previously Presented) The system of claim 104 wherein the device processor attempting to change the state of the bus includes the device processor forcing a state on the bus.

106. (Previously Presented) The system of claim 105 wherein the device processor forcing the state of the bus includes the device processor transmitting one of a digital high value and a digital low value on the bus.

107. (Previously Presented) The system of claim 105 further comprising the device processor reading the bus after attempting to affect the bus, wherein the device processor determines the inability to affect the bus using the reading of the bus.

108. (Previously Presented) The system of claim 91 further comprising the device processor performing further fault detection upon severing of the communication link, wherein when the device processor detects no device fault from the further fault detection, the device processor reestablishes the communication link with the bus.

109. (Previously Presented) The system of claim 91 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising the I/O device being assigned to one of the synchronous time slots, where the device processor performs fault detection during the asynchronous time slot following the corresponding synchronous time slot.

110. (Previously Presented) The system of claim 91 wherein the device processor performs the fault detection when the I/O device is not transmitting I/O device information on the bus.